Single Event Transient and Single Event Upset

electrical simulation under Cadence

based on MUSCA SEP

3 current sources

in 0.18/0.35 CIS process

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CNES Workshop “Radiation Effects on Optoelectronics Detectors”

November 26th 2014
Outline

- *Introduction on radiation and Single Events*
- Current generation mechanisms and Soft Error in sequential electronics
- Presentation of the approach
- AND cell ⇌ SET study
- Register (DFF) ⇌ SEU study
- Conclusion and perspective
Introduction on radiation and Single Events
Radiation space environment (Esa slide, A. Fernández-León)

Radiation Effects in semiconductor devices

- Terrestrial, Atmospheric, Nuclear energy
  - X-rays
  - γ-rays
  - Electromagnetic radiation

- Trapped particles (Van Allen Belts)
  - Neutrons
  - Electrons
  - Protons
  - Heavy ions

- Galactic rays, Solar particles
  - α-rays
  - High energy photons

TOTAL IONISING DOSE EFFECTS

DISPLACEMENT DAMAGE EFFECTS

SINGLE EVENT EFFECTS

⇒ Cumulative effects
⇒ Dose effects ∆ oxide thickness
  ⇒ Vt shifts (reduced <0.35um)
⇒ Noise & leakage (Dark Current)

⇒ Instantaneous effects,
⇒ SEL Single Event Latchup
  ⇒ can be destructive, power off req.
⇒ SEU Single Event Upset
⇒ SET Single Event Transient
⇒ SEU + SET lead to Soft Error and SEFI
Introduction on radiation and Single Events

Example of SEE counter measures:

**e2V CIS for MTG-FCI VisDA (prime TAS-F for ESA, EUMETSAT)**

- **Imager with analog outputs**
- **Specific Layout (DRC) to SEE tolerance**
- **Archi. : Triple Modular Redundancy**
- **Heavy ions tests have shown:**
  - No Latch Up up to 67.7 MeV.cm$^2$/mg
  - No SEFI up to 67.7 MeV.cm$^2$/mg
  - Soft Error rate drastically reduced comparing to regular standard cells

- Complicated work to test and assess the SEE tolerance (requires monitoring chip under beam !)
- All results (fortunately very promising) come after the design phase...
- This talk aims to propose an alternative way to emulate heavy ions during design phase
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Current gen. mechanisms and SE in sequential electronics

**Principle of SET generation : CMOS inverter case**

- **Diffusions** (drains and sources of MOS transistor) ⇒ separate pairs (built in field)
- Ion strike on OFF transistor drains, only, can lead to dangerous transients

**Ion strike on drain of a PMOS :**

P+/Nwell diffusion

- Positive pulse (V) on a 0
- Drain PMOS @1 (ON) ⇒ no consequence
- Drain PMOS @0 (OFF) ⇒ 0 interpreted as 1

**Ion strike on drain of a NMOS :**

N+ /Pwell diffusion

- Negative pulse (V) on a 1
- Drain NMOS @1 (OFF) ⇒ 1 interpreted as 0
- Drain NMOS @0 (ON) ⇒ no consequence

- Positive/Negative voltage pulse generated resp. on PMOS/NMOS drain

- SET can be shaped in and transmitted by circuitry
Current gen. mechanisms and SE in sequential electronics

**Soft errors in sequential logic**

- SET can propagate in combinatorial logic...
- ...and **might** *(might not: timing/duration, amplitude)* produce error

- **Soft errors** originate from SET *and* SEU
- Ck (or Reset) **should be treated**, gravity high but assoc. circuitry area small (lower probability)
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Presentation of the approach

Methodology: Musca (current calc.) + Cadence (electrical simu.)

- **Process Deck:** Foundry, ITRS
- **GDSII File**
- **MUSCA**
  - Scanned Area definition
  - Heavy ion strike
  - Current sources generation
- **Ion characteristics**
  - LET, incidence angle...
- **Scanned Area** (around drains)
- **Current sources**
- **Batch of electrical simulation (Spectre)**
- **Processing**
- **Cadence**
- **Impact points producing SEU**
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AND cell ⇒ SET study
SET results on AND cell

- Electrical simulation:
  - 3V3 standard cell loaded with 2 NAND
  - Parasitic view of the cell simulation
  - Static simulations (No input changes when ion strikes)

![Diagram of AND cell with SET results]

Voltage (V)

Threshold

Negative/positive pulse: SET “greater” than threshold

© e2v
AND cell $\Rightarrow$ SET study

SET Number of glitches vs threshold for AND cell

- localization of ions impacts vs SET amplitude (V)

<table>
<thead>
<tr>
<th>Threshold (V)</th>
<th>LET (MeV cm²/mg)</th>
<th>Threshold (V)</th>
<th>LET (MeV cm²/mg)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>10</td>
<td>10</td>
<td></td>
</tr>
<tr>
<td>0.1</td>
<td></td>
<td>20</td>
<td></td>
</tr>
<tr>
<td>0.5</td>
<td></td>
<td>30</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>60</td>
<td></td>
</tr>
</tbody>
</table>

- Cumulative mapping for inputs (0,0); (0,1); (1,0); (1,1)
AND cell ⇒ SET study

Inputs logic level influence on pulse duration
(LET 60MeV.cm²/mg)

Slider bar: A=1, B=0

SET duration histogram at the output of the 2nd NAND

<table>
<thead>
<tr>
<th>BA=00</th>
<th>BA=01</th>
<th>BA=10</th>
<th>BA=11</th>
</tr>
</thead>
<tbody>
<tr>
<td><img src="image1" alt="Graph" /></td>
<td><img src="image2" alt="Graph" /></td>
<td><img src="image3" alt="Graph" /></td>
<td><img src="image4" alt="Graph" /></td>
</tr>
</tbody>
</table>

Large SET only in this case

Width @ Vdd/2

© e2v
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Register (DFF) ⇒ SEU study

Presentation of the cell

- Symbol and principle schematic (ck is high), loaded for elec. simulations

- Static simu. ⇒ data + clock unchanged during ion strike

- Layout ⇒
Register (DFF) ⇒ SEU study

SEU in latch1 (stg1) of the register when clock is High

- Area corrupted (SEU) is dependent of:
  - clock state mem. state or opened write state
  - value memorized (1 or 0)
- Ion strikes: pairs drift and separate in stg1 NMOS diffusion
  - negative current
  - negative SET + Feed Back
- Corruption of 1! (1 changed in a 0): propagates to out
Register (DFF) $\Rightarrow$ SEU study

Electrical curves when clock is high

SEU occurred!

$\text{current}$

$\text{stg1}$

$\text{stg2}$

$\text{out}$

$\text{time(ns)}$
Register (DFF) ⇒ SEU study
Number of SEU versus low LET

- LET 10 MeV.cm²/mg
  - Only NMOS diff. sensitive!
  - Overlapping SEU Clk_High/Clk_Low

- LET 20 MeV.cm²/mg
  - Overlapping SEU Clk_High/Clk_Low
Register (DFF) ⇒ SEU study
Number of SEU versus high LET

- LET 30 MeV.cm²/mg
  - 1 to 0
  - 0 to 1

- LET 60 MeV.cm²/mg
  - 1 to 0
  - 0 to 1
Register (DFF) ⇒ SEU study
SEU cross section comparison : Musca & Electrical Simu. vs Measure

- Measurement on this register (BER on scan of 376 registers) to compare with simulation:

![](slide)

- Simulation Fits pretty well (except @ low LET)
  ⇒ @ low LET 10000 ions/sec/cm² (and 1MHz clock) : physical calibration Musca to get absolute tool
  ⇒ Scan area should be enlarged (underestimation of saturation cross section)
Register (DFF) ⇔ SEU study

Increasing the LET threshold to SEU

- Increasing **capacitance (+7fF)** (netlist) on critical nets
  ⇔ improve SEU th. but degradation in maximum speed...

- LET 10 MeV.cm²/mg (without capacitors)

- LET 10 MeV.cm²/mg (**with capacitors**) : no more events
Register (DFF) ⇒ SEU study
Increasing the threshold to SEU

- Cross section comparisons

- Threshold with capacitors above 10MeV.cm²/mg with cap.
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Conclusion …

• Predictive Chain for Soft Error caused by Heavy ions developed through: and e2V collaboration

• “Good” agreement ⇒ SEU X-sections simu. vs measurement

• Sensitive areas can be identified
  ⇒ treatment checked
  ⇒ relative tool need calibration

• Better understanding of Soft Error mechanisms…
... and perspectives

- Enabling effective SET-SEU rad-hardening validation before Silicon
  - Validation of mitigation techniques at gate level
  - Should be used at design start!

- Approach’s flexibility enables quantifying (roughly) process changes
  - EPI thickness (e.g. QE improvement)
  - other CMOS processes

- SEU/SET rad-hard cells development with this tool
  - silicon tests soon

- Benefit for future e2V space products hardening
  - e.g. charges transfer CMOS TDI (pixel performances silicon proven today)

Thank you for your attention!